2003 GaAs MANTECH

International Conference on Compound Semiconductor Manufacturing Technology

Organizers: GaAs MANTECH, Inc., Campus Box 1127
One Brookings Drive, St. Louis, MO 63130-4899, USA
Tel: +1 314-935-5575
E-mail: info@gaasmantech.org www.gaasmantech.org

May 19-22, 2003
Marriott Camelback Inn Resort, Golf Club & Spa
5402 E. Lincoln Drive, Scottsdale, AZ 85253 USA
Tel: +1-800-242-2635

Once again GaAs MANTECH (with III-Vs Review acting as media sponsor) promises to deliver high quality papers covering all aspects of compound semiconductor manufacturing, with speakers from leading-edge equipment, epiwafer, and device suppliers. Since its launch in 1986, GaAs MANTECH has consistently been one of the highlight events of the conference calendar. Coverage includes all compound-based semiconductors, not just GaAs. With an excellent technical program comprising of almost 80 papers and expanded workshop sessions, the 2003 event should prove the best ever. As in previous years, an Interactive Forum and Ugly Picture Contest will be included. A major attraction will be the associated exhibition, with more than 70 suppliers expected to participate.

Exhibitors (registered as of February 2003)

Accent Optical Technologies
AIXTRON, Inc.
American Xtal Technology
ASML Special Applications
BOC Edwards
Compound Semiconductor Magazine
EMCORE Corporation
EpiWorks, Inc.
EV Group, Inc.
Evans Analytical Group
Freiberger Compound Materials USA
Frontier Semiconductor
General Chemical Corporation
Hitachi Cable America, Inc.
Hologenix, Inc.
III-Vs Review
INFICON
Intelligent Epitaxy Technology
IQE, Inc.
JMAR/SAL NanoLithography, Inc.
Kopin Corporation
Lake Shore Cryotronics
MBE Technology Pte., Ltd.
Panalytical (Philips Analytical, Inc.)
Praxair Electronics
PROCOMP Informatics Ltd.
RIBER
SAES Pure Gas, Inc.
Semitool, Inc.
Solid State Equipment Corp.
Sumitomo Electric Semiconductor Materials, Inc.
SUNTEK Compound Semiconductor Co., Ltd.
Surface Technology Systems plc
Tegal Corporation
Temescal (unit of the BOC Group, Inc.)
Trikon Technologies, Inc.
Unaxis USA Inc.
Vacuum Engineering & Materials Co.
Veeco - Applied Epi

Conference Agenda - at a glance

Sunday, May 18		
Registration	5:00pm - 9:00pm	Arizona Reg. Desk
Monday, May 19		
Registration	7:00am - 10:00am	Arizona Reg. Desk
Buffet Breakfast	7:00am - 8:00am	Peace Pipe
Workshops	8:00am - 5:00pm	Sunshine/Cholla
Workshop Luncheon	11:45am - 1:00pm	Sonoran Terrace
Registration	12:00pm - 8:00pm	Arizona Reg. Desk
Exhibits Reception	6:00pm - 9:00pm	Arizona Ballroom
Tuesday, May 20		
Registration	7:00am - 5:30pm	Arizona Reg. Desk
Continental Breakfast	7:00am - 8:00am	Arizona Ballroom
Session 1: *Plenary*	8:00am - 9:50am	Sunshine/Cholla
Break	9:50am - 10:20am	Arizona Ballroom
Exhibits open	9:50am - 4:00pm	Arizona Ballroom
Session 2: *Devices I*	10:20am - 11:50am	Sunshine/Cholla
Exibits Lunch	11:50am - 1:10pm	Arizona Ballroom
Session 3: *Materials*	1:10pm - 3:00pm	Sunshine/Cholla
Break	3:00pm - 3:30pm	Arizona Ballroom
Session 4: *Dielectrics & Capacitors*	3:30pm - 5:30pm	Sunshine/Cholla
International Reception	6:00pm - 10:00pm	Mummy Mountain
Wednesday, May 21		
Registration	7:00am - 11:00am	Arizona Reg. Desk
Continental Breakfast	7:00am - 8:00am	West Foyer
Session 5: *Packaging*	8:00am - 9:50am	Sunshine/Cholla
Break	9:50am - 10:10am	West Foyer
Session 6: *Metallization*	10:10am - 11:50am	Sunshine/Cholla
Awards Lunch	11:50am - 1:10pm	Sonoran Terrace
Registration	1:00pm - 5:00pm	Arizona Reg. Desk
Session 7: *Devices II*	1:10pm - 3:10pm	Sunshine/Cholla
Break	3:10pm - 3:30pm	West Foyer
Session 8: *Interactive Forum/Ugly Pictures*	3:30pm - 5:30pm	Arizona Ballroom
Session 9: *Rump Sessions*	6:00pm - 7:30pm	Arizona Ballroom
SEMI Standards Meeting	7:30pm - 9:00pm	Exec. Board Room
Thursday, May 22		
Registration	7:00am - 9:00am	Arizona Reg. Desk
Continental Breakfast	7:00am - 8:00am	West Foyer
Session 10: *Backside Processing*	8:00am - 10:00am	Sunshine/Cholla
Break	10:00am - 10:20am	West Foyer
Session 11: *Devices III*	10:20am - 12:00pm	Sunshine/Cholla
Lunch	12:00pm - 1:10pm	Attendees' Choice
Session 12: *Advanced Processes & Methods*	1:10pm - 2:50pm	Sunshine/Cholla
Break	2:50pm - 3:10pm	West Foyer
Session 13: *Wide Band Gap Technologies*	3:10pm - 5:10pm	Sunshine/Cholla
Ugly Picture Finals	5:30pm - 6:30pm	Arizona Ballroom
Conference Close	6:30pm	

Full Technical Programme

Monday, May 19

WORKSHOP (Chair: J. Crites, *MIA–COM*)

8:00am	**Welcome/Introductions**	OR	
8:15am	**IC Processing Tutorial: Materials**	8:15am	**Wireless for Dummies: Part 1**
9:30am	**IC Processing Tutorial: Patterning**	9:30am	**Wireless for Dummies: Part 2**
10:45am	**IC Processing Tutorial: Metallization**	10:45am	**Poweramps for Wireless Applications**
1:00pm	**Micro–Electrical–Mechanical Systems (MEMS)**	1:00pm	**GaN**
3:15pm	**SiGe Processing Overview**	3:15pm	**Advanced Interconnect**

Tuesday, May 20

8:00am **Welcoming Ceremonies** (B. Surridge, *Nortel Networks*, Conference Chair)

8:10am **Technical Program Highlights** (Chun–Lim Lau, *Booz Allen Hamilton*, Program chair)

SESSION 1: PLENARY (Chair: Chun–Lim Lau, *Booz Allen Hamilton*)

8:20am **The Trend in the Wireless Market, Products and Business** (D. Aldrich, *Skyworks Solutions, Inc.*)

8:50am **DARPA Perspective on the Future of Electronics** (J. Zolper, *DARPA/MTO*)

9:20am **GaAs and SiGeC BiCMOS Cost Comparison – Is SiGeC Always Cheaper?** (M. Wilson, *Motorola, Inc.*)

SESSION 2: DEVICES I – Technology Overview & Novel Devices (Chair: C. Della–Morrow, *Motorola, Inc.*)

10:20am **Advance of Compound Semiconductors in China** (J. Zhou and Q. Huang, *Chinese Academy of Sciences & Advanced Chinese Epitaxy Ltd.*)

10:50am **RF Poweramplifiers for Cellphones** (C.E. Weitzel, *Motorola, Inc.*)

11:10am **Ultra Broadband MEMS Switch on Silicon and GaAs Substrates** (R. Chan, R. Lesnick, D..Caruth, and M. Feng, *University of Illinois*)

11:30am **Root Cause Analysis and Reduction of Off–State Leakage Current to Increase Manufacturability of a HIGFET Device** (J. Hughes, E. Huang, J. Apibunyopas, C. Della, T. Nilsson, and M. Coe, *Motorola, Inc.*)

SESSION 3: MATERIALS (Co–Chairs: P. Cooke, *Emcore* and R. Kremer, *Freiberger Compound Materials*)

1:10pm **Impact of Substrate Imperfections on MBE Epitaxial Layer Quality** (M. Wojtowicz, R. Sandhu, R. Tsai, and T. Block, *Northrop Grumman Space Technology*)

1:40pm **Use of Re–etched and Re–polished Epi–wafers for MBE Calibration Substrates** (J. Lowmaster, R. Pelzel, M. Dydyk, D. Green, *IQE Inc.*)

2:00pm **Commercial Production of Large Diameter InP–HBT Epiwafers by MBE** (D.I. Lubyshev, K. Teker, Y. Wu, J.M. Fastenau, X.–M. Fang, C. Doss, A.B. Cornfeld, and W.K. Liu, *IQE Inc.*)

2:20pm **Volume Epitaxial Growth of Enhanced Mode HIGFETs using Minimal Material Characterization and Rapid Inline Processing to Minimize Risk** (M. Pelczynski, M. Rittgers, B. Duffin, C. Della, and M. Mikhov, *Motorola, Inc. & Arizona State Univ.*)

2:40pm **Active Carbon Control During the VGF Growth of Semi–insulating GaAs** (J. Stenzenberger, T. Bünger, M. Jurisch, F. Börner, U. Kretzer, S. Eichler, R. Bindemann, B. Weinert, S. Teichert, and T. Flade, *Freiberger Compound Materials GmbH*)

SESSION 4: DIELECTRICS & CAPACITORS (Chair: M. Bourke, *Trikon Technologies*)

3:30pm **MIM's the Word – Capacitors for Fun and Profit** (M. Brophy, A. Torrejon, S. Petersen, K. Avala, and L. Liu, *TriQuint Semiconductor*)

3:50pm **On the Development of High Density Nitrides for MMICs** (Y.C. Chou, R. Lai, G.P. Li, R. Grundbacher, H.K. Kim, P. Nam, Y. Ra, Q. Xu, M. Barsky, M. Biedenbender, and A. Oki, *Northrop Grumman Space Technology, UC Irvine & Bethel Material Research*)

4:10pm **Development and Characterization of a 600Å PECVD Si3N4 High–Density MIM Capacitor for InGaP/GaAs HBT Applications** (J. Yota, R. Ramanathan, J. Arreaga, P. Dai, C. Cismaru, R. Burton, P. Bal, and L. Rushing, *Skyworks Solutions, Inc.*)

4:30pm **Characteristics of Low–k Film Deposited by Plasma–enhanced CVD using a Liquid BCB Source** (S. Sugitani, H. Matsuzaki, and T. Enoki, *NTT Photonics Laboratories*)

4:50pm **Metal Particle Effects on Thin Film Capacitors in High Volume Manufacturing** (M. R. Rao, S. T. O'Neil, S. Tiku, *Skyworks Solutions, Inc.*)

5:10pm **Backside Emission Microscopy Applications in Compound Semiconductor Manufacturing Debug** (H. Henry, D. Hill, M. Sadaka, P. Sanders, and S. Wilson, *Motorola*)

Wednesday, May 21

SESSION 5: PACKAGING (Chair: H. Knoedler, *Skyworks Solutions, Inc.*)

8:00am **Compact System–on–Package (SOP) Architecture for Low Cost RF Front–end Module** (J.Laskar, S. Pinel, K. Lim, M.F. Davis, M. Maeng, R. Li, and M. Tentzeris, *Georgia Institute of Technology*)

8:30am **Integrated Circuit using Embedded III–V–on–Ge MHEMTs in Multi–layer Thin–film Technology** (R. Vandersmissen, D. Schreurs, S. Vandenberghe, G. Carchon, and G. Borghs, *IMEC & K.U.Leuven.*)

8:50am **Wafer–Scale Assembly of Heterogeneous Technologies** (J.–Q. Lu, A. Jindal, P.D. Persans, R.J. Gutmann, *Rensselaer Polytechnic Institute*)

9:10am **Dense, Two–Dimensional Optoelectronic Chips for High–Speed, Parallel Optical Links** (D. Burrows, K. Zabierek, R. Dennis, S. Wade, and R. Cook, *TeraConnect, Inc.*)

9:30am **Power GaInP/GaAs HBTs for High Voltage Operation** (P. Kurpas, A. Maaßdorf, W. Doser, W. Köhler, P. Heymann, B. Janke, F. Schnieder, H. Blanck, P. Auxemery, D. Pons, W. Heinrich, and J. Würfl, *Ferdinand–Braun–Institut für Höchstfrequenztechnik & United Monolithic Semiconductors*)

SESSION 6: METALLIZATION (Chair: M. Young, *RF Micro Devices*)

10:10am **Refractory Gate Metallization Characterization for EMODE 2 Poweramplifiers** (James Cotronakis, Thomas K. Nilsson, *Motorola, Inc.*)

10:30am **Fabrication and Characterization of Thin Film Resistors for GaAs–Based Poweramplifiers** (H. Shen, J. Arreaga, R. Ramanathan, H. Knoedler, J. Sawyer, and S. Tiku, *Skyworks Solutions, Inc.*)

10:50am **NiGeAu Ohmic Contact in InGaP PHEMTs** (E. Lan, Q. Xie, P. Fejes, and H. Le, *Motorola, Inc.*)

11:10am **Advances in Gold Metallization at Motorola's Compound Semiconductor Fab (CS1)** (C. Becker, W. Rummel, P. Ocansey, *Motorola, Inc.*)

11:30am **The Study of Dendrites Formation Mechanism to Enhance Gold Plating Process Yield, Throughput, and Solution Lifetime** (S.J. Huang, H.C. Chou, T.C. Lee, B. Lin, D.W. Tu, P.C. Chao, and C.S. Wu, *WIN Semiconductors Corporation*)

SESSION 7: DEVICES II – Technology Overview & FET Devices (Chair: N. Pan, *Microlink Devices*)

1:10pm **High Voltage Microwave Devices: An Overview** (D. Miller and M. Drinkwine, *MIA–COM*)

1:40pm **Rapidly Developing Compound Semiconductor Technology and Industry in Taiwan** (Y. Liu, *Industrial Technology Research Institute, Taiwan*)

2:10pm **High Speed 0.18mm Ion–implanted GaAs MESFET Process with High Uniformity & Excellent Reproducibility** (D. Fukushi, M. Watanabe, and S. Nakajima, *Sumitomo Electric Ind., Ltd.*)

2:30pm **Deterministic Process Control using a Multivariate Model** (D. Miller, *MIA–COM*)

2:50pm **Trade–off Relationship between Breakdown and Gate–Lag in Recessed–Gate GaAs FETs** (Y. Mitani, D. Kasai, and K. Horio, *Shibaura Institute of Technology (Japan)*)

SESSION 8: INTERACTIVE FORUM and UGLY PICTURE CONTEST (Co–Chairs: K. Alavi, *BAE Systems*, and O. Tal, *MAX International Engineering Group*)

3:30pm – 5:30pm:

8.1 **Optimization of PHEMT for Microwave Power Applications** (T. Baksht, S. Solodky, and Y. Shapira, *Tel Aviv University & Gal–El (MMIC)*)

8.2 **The First 0.15mm MHEMT 6" GaAs Foundry Service: Highly Reliable Process for 3 V Drain Bias Operations** (M. Chertouk, W.D. Chang, C.G. Yuan, H.H. Chen, L. Lo, C.H. Chen, D.W. Tu, J. Liu, N. Draidia, and P.C. Chao, *WIN Semiconductors Corp.*)

8.3 **High Power Ka–Band PIN Diode Technology** (B. Houli–Arbiv, G. Bunin, J. Kaplun, I. Hallakoun, T. Boterashvili, Y. Knafo, A. Cohen–Nov, M. Leibovitch, and B. Revzin, *Gal–El (MMIC)*)

8.4 **Predictive Modeling of InGaP/GaAs HBT Noise Parameters from DC and S–Parameter Data for Wireless Poweramplifier Design** (J. Chingwei Li, P. Zampardi, and V. Pho, *UCSD & Skyworks Solutions, Inc.*)

8.5 **Intermetallic Phase Formation in Gold–Tin Alloys Electroplated from a Non–cyanide Bath** (Y. Zhang, D. Ivey, *University of Alberta*)

8.6 **Cycle Time Reduction During Electroplating of Through Wafer Vias For Backside Metallization of III–V Semiconductor Circuits** (D. Anderson, H. Knoedler, and S. Tiku, *Skyworks Solutions, Inc.*)

8.7 **Properties, Process Control, and Characterization of PECVD Silicon Nitrides for Compound Semiconductor Devices** (C.S. Cook, T.K. Daly, R. Liu, M. Canonico, M. Erickson, Q. Xie, R.B. Gregory, and S. Zollner, *Motorola, Inc. & Arizona State Univ.*)

8.8 **Characterization and Control of Galvanic Corrosion During GaAs Wafer Photoresist Processing** (J. Moore, H. Hendriks, and C. Varmazis, *General Chemical & MIA–COM*)

8.9 **Low Damage Dielectric Etching on GaAs Using a Helicon Wave High Density Source** (F.S. Pool, W.A. Wohlmuth, E. Maxwell, B. Berggren, S. Roadman, S. Mahon, B. Howell, and W. Mickanin, *TriQuint Semiconductor*)

8.10 **Improved Etch Process Control of TiWN Gate Length** (J. Fender, J. Hill–Tinkler, and S. Chorrushi–Patino, *Motorola, Inc.*)

8.11 **Life Tests and TDDB Life Prediction Modeling of 50 nm Silicon Nitride Capacitors** (G. Drandova, J. Beall, K. Decker, and K. Salzman, *TriQuint Semiconductor*)

8.12 **Process Optimization for 0.5 µm Dual Recess PHEMT Poweramplifiers** (S. Nayak, M. King, K. Salzman, and J. Beall, *TriQuint Semiconductor*)

8.13 **Comparison of InAlAs/InP Hetero–interface Properties – MBE vs. MOCVD** (M. Takakusaki, H. Momoi, K. Kakuta, and H. Nakata, *Nikko Materials Co., Ltd.*)

8.14 **Development of High Gain and High Efficiency InGaP/GaAs HBT for High Voltage Operation** (Y. Yang, K. Feng, B. In, C. Nguyen, D. Hou, Y. Chen, and D. Wang, *GCS, Inc.*)

8.15 **Strength Improvement for the GaAs Thin Wafer** (H. Pham, C. Hua, and Q. Luo, *Skyworks Solutions, Inc.*)

8.16 **Anisotropic and Smooth Etching of In–containing Multi–layer Structures Using ICP Plasma for Optoelectronic Devices Manufacturing** (Y. Lee, M. DeVre, B. Reelfs, D. Lishan, and R. Westerman, *Unaxis USA, Inc.*)

8.17 **Yield Enhancement Using Final Outgoing Automated Inspection System** (K. Lenaburg, S. Valocchi, and J. Campbell, *Motorola, Inc.*)

8.18 **A Comparison of BCB with Polyimide Process in Manufacturing HBT Devices** (J. Nguyen, O. Dydasco, H. Saigusa, and C. Hua, *Novalux, Inc. & Skyworks Solutions, Inc.*)

8.19 **Building Solder Bumps on GaAs Flip Chip Schottky Devices** (P. Sricharoenchaikit, *MIA–COM*)

8.20 **Stress and Other Challenges with Evaporated Ni–Cr Thin Film Resistors Used in the Manufacture of ASICs** (Necmi Bilir and Long Do, *Skyworks Solutions, Inc.*)

8.21 **Optical Device Wafer Manufacturing in an IC Foundry** (S. Wang, G. Feng, S. Lee, S. Wang, and C. Nguyen, *GCS, Inc.*)

8.22 **Improving Process Yield by Utilizing Smart SPC Rules** (O. Tal, *MAX International Engineering Group*)

8.23 **High Yield Lithography and Wafer Handling Methods for Reliable Backside Processing of Brittle III–V Materials** (C. Schaefer, V. Dragoi, S. Farrens, M. Wimplinger, and P. Lindner, *EV Group Inc.*)

8.24 **An InP/InGaAs SHBT Technology for High–Speed Monolithic Optical Receivers** (S. Shen, D. Caruth, D. Chan, A. Thu, and M. Feng, *Xindium Technologies, Inc.*)

8.25 **Advanced Commercial InP HBT IC Process** (X. Nguyen, J. Fierro, K.T. Feng, and C. Nguyen, *GCS, Inc.*)

8.26 **Improved Characterization of AlGaAs Laser Diode using Backside SIMS** (P. Lierde and C. Tian, *Charles Evans & Associates*)

SESSION 9: RUMP SESSIONS (Co–Chairs: M. Young, RF Micro Devices, and M. Barsky, *Northrop Grumman Space Technology*)

6:00pm – 7:30pm:

- **Next Killer Applications**
- **Is GaAs Toast? – The future, or lack thereof, of GaAs (back by popular demand)**
- **Cost Reduction Strategies**
- **The Future: Wide Bandgap Devices?**
- **Is Optoelectronics Manufacturable?**

Thursday, May 22

SESSION 10: BACKSIDE PROCESSING (Chair: P. Werbaneth, *Tegal Corporation*)

8:00am **New Manufacturing Concepts for Ultra–Thin Silicon and Gallium Arsenide Substrates** (K. Bock, M. Bleier, O. Köthe, and C. Landesberger, *Fraunhofer Institute for Reliability and Microintegration IZM–M*)

8:20am **A Novel Backside Process to Achieve 1–mil Thick Wafers at 6–inch Foundry** (H.C. Chou, T.C. Lee, S.J, Huang, H.H. Weng, M.H. Tsai, D.W. Tu, M. Chertouk, J.M. Lee, P.C. Chao, and C.S. Wu, *WIN Semiconductors Corporation*)

8:40am **Impact of Backside Via Dimension Changes on High Frequency GaAs MMIC Circuit Performance** (P. Nam, R. Tsai, M. Barsky, R. Grundbacher, R. Lai, S. Olson, D. Davison, and B. Allen, *Northrop Grumman Space Technology*)

9:00am **Dry Etching of Deep Backside Vias in InP** (M. Huffman, T. Engel, N. Pfister, G. Arevalo, T. Brown, M. Farhoud, R. Miller, B. Keppeler, J. Staroba, and R. Jefferies, *Agilent Technologies Inc. & Trikon Technologies Ltd.*)

9:20am **Eliminating Pillars During GaAs Via Etch** (R. Westerman, D. Johnson, and F. Clayton, *Unaxis USA, Inc. & Motorola, Inc.*)

9:40am **Optimization of Metal Adhesion for GaAs Backside Wafer Processing** (T. Daly, J. Fender, B. Duffin and M. Kottke, *Motorola, Inc.*)

SESSION 11: DEVICES III – HBTs & InP Devices (Chair: D. Green, *IQE Inc.*)

10:20am **Activities of Indium Phosphide in Japan** (Y. Miyamoto and Y. Tohmori, *Tokyo Institute of Technology & NTT Photonics Laboratories.*)

10:50am **The Emergence of SiGe:C HBT Technology for RF Applications** (V. Ilderem and S. Thomas, *Motorola, Inc.*)

11:20am **Investigation of Stressing InP/InGaAs DHBTs under High Current Density** (V.E. Houtsma, J. Frackoviak, R.F. Kopf, R.R. Reyes, W. Sung, A. Tate, J. Tong, Y. Yang, N.G. Weimann, and Y.K. Chen, *Lucent Technologies*)

11:40am **GaInP/GaInAsN/GaAs N–p–N Bipolar Transistors: Influence of Base Layer Composition and Alloy Grading on Device Performance** (B. Dickerson, B. Heath, and L. Guido, K. Stevens, C. Lutz, E. Rehder, and R. Welser, *Virginia Polytechnic Institute and State University & Kopin Corporation*)

SESSION 12: ADVANCED PROCESSES & METHODS (Chair: M. Sherwin, *Emcore – EPI/EOD*)

1:10pm **In–Line Defectivity Methodology for a GaAs Manufacturing Facility** (J. Campbell, K. Lenaburg, and N. Liggins, *Motorola, Inc.*)

1:30pm **High Uniformity, Highly Reproducible Non–selective Wet Gate Recess Etch Process for InP HEMTs** (Xin Cao, and Iain Thayne, *University of Glasgow*)

1:50pm **A High Performance and High Yield Self–Aligned and Double Recessed pHEMT Process with One Lithography Step for Both Gate and First Recess Definition** (K. Tabatabaie Alavi, C. Whelan, and E. Tong, *Raytheon RF Components*)

2:10pm **Electrophoretic Photoresist Application for High Topography Wafer Surfaces** (J. Tajadod, H. Dendriks, J. Klocke, A. Morales, and H. Rapuano, *MIA–COM*)

2:30pm **Advances in CPL, Collimated Plasma Source & Full Field Exposure for Sub–100nm Lithography** (B. Boerger, S. Mcleod, and R. Forber, *JMAR/SAL Nanolithography*)

SESSION 13: WIDE BANDGAP TECHNOLOGIES (Chair: E. Delhaye, *Philips Semiconductors*)

3:10pm **Ti/Al/Ni/Au Ohmic Contacts on AlGaN/GaN HEMTs** (A. Crespo, R. Fitch, J. Gillespie, N. Moser, G. Via, and M. Yannuzzi, *AFRL/SND Wright Patterson AFB*)

3:30pm **AlGaN/GaN HEMTs on Silicon Carbide Substrates for Microwave Power Operation** (R. Lossy, P. Heymann, J. Würfl, N. Chaturvedi, S. Müller and K. Köhler, *Ferdinand–Braun–Institut für Höchstfrequenztechnik & Fraunhofer–Institut für Angewandte Festkörperphysik*)

3:50pm **GaN–HEMT on 100mm Diameter Sapphire Substrate Grown by MOVPE** (Y. Otoki, M. Kihara, T. Tanaka, K. Takano, T. Kikkawa, and T. Igarashi, *Hitachi Cable, Fujitsu Laboratories Ltd. & Fujitsu Quantum Devices Ltd.*)

4:10pm **Transition of High Power SiC MESFETs from 2–inch to 3–inch Production for Improved Cost and Producibility** (J.W. Milligan, S.T. Allen, J. Sumakeris, A.R. Powell, J. Jenny, and J.W. Palmour, *Cree, Inc.*)

4:40pm **Solid–State Lighting: Lamp Targets and Implications for the Semiconductor Chip** (J. Tsao, *Sandia National Laboratories*)

5:30pm **UGLY PICTURE CONTEST FINALS** (Chair: B. Surridge, *Nortel Networks Optical Components*)

6:30pm **Close**